REMARKS

Claims 53-54, 56-67, 69-78 and 80-88 are pending in the application.

Claims 53-54, 56-67, 69-78 and 80-88 stand rejected.

In light of the following remarks, applicant respectfully requests reconsideration and reexamination of all pending claims

Rejection of Claims under 35 U.S.C. § 103

Claims 53-54, 56-66, 69-78 and 80-88 stand rejected under 35 U.S.C. § 103 as being unpatentable over Tanaka et al., U.S. Patent 4,910,667 (Tanaka), in view of Birrittella et al., U.S Patent 6,266,759 (Birrittella).

With respect to the references cited, Applicant respectfully notes that Tanaka, in view of Birrittella, fails to show, teach, or suggest the limitations of claim 53 of the claimed invention. Claim 53 includes:

> generating a vector transfer unit exception ***if a second program*** attempts to transfer vector data between memory and a register of the register file via any vector buffer of the vector buffer, if said configuration register indicates that said vector buffer is in use.

The office action (paper 10) dated June 20, 2003 admits that Tanaka fails to teach or suggest the limitation set forth above. The final office action (paper 16) dated February 12 maintains the rejections of paper 10. As such, the final office action admits that Tanaka fails to teach or suggest the limitation above. Further, Tanaka discloses a vector buffer storage system that transfers data between main storage and a vector buffer

in response to a vector data instruction. (column 2, lines 9-12). The vector data instruction initiates the vector data transfer, which is different from a program initiating the vector data transfer. In focusing on using a vector data instruction to initiate the vector data transfer, Tanaka does not appear to discuss the possibility of more than one program attempting to transfer vector data in column 2, lines 9-12. Therefore, column 2, lines 9-12 of Tanaka does not show, teach, or suggest "generating a vector transfer unit exception if a second program attempts to transfer vector data between memory and a register...if said configuration register indicates that said vector buffer is in use," as recited in claim 53.

The final office action alleges via paper 10 that Birrittella discloses the limitation of claim 53 set forth above. Claim 53 requires "generating a vector transfer unit ***exception*** if a ***second program*** attempts to transfer vector data." The final office action focuses on the "exception" limitation while ignoring the "second program" limitation.

Birrittella teaches a system that "stalls all instructions currently executing" if a second instruction attempts to access a vector buffer while an indicator is in the live state. Birrittella teaches that instructions, not programs, can attempt to access a vector buffer. (column 5, line 56 to column 6, line 9). Clearly, column 6, lines 2-9 of Birrittella does not teach or fairly suggest "generating a vector transfer unit exception if a second program attempts to transfer data between memory and a register of the register file via any vector buffer of the vector buffer pool if said configuration register indicates that said vector buffer is in use," either alone or in combination with the remaining limitations recited in claim 53.

Additionally, Applicant is unable to find anywhere in Tanaka or Birrittella the motivation to combine their disclosures to provide the advantages of the present invention. This is likely due, at least in part, to the fact that neither reference appears to recognize the problem solved by the present invention.

Tanaka points out that memory access times are slower when the vector buffer is temporally distant from the vector registers and the main storage. Tanaka proposes to solve this problem by placing the vector buffer between the vector registers and the main storage. (column 2, lines 21-43). Thus, Tanaka provides a hardware solution to a hardware problem. Problems that arise with respect to handling multiple programs are usually addressed at an operating system level, not a hardware level. Tanaka does not appear to address issues involving operating systems, and therefore fails to recognize the need to address the problems that arise when a second program attempts to transfer vector data between memory and a register reserved by a first program. Therefore, one of skill in the art would find no motivation in Tanaka to look to any other reference, including Birrittella, to provide for generating a vector transfer unit exception if a second program attempts to transfer vector data between memory and a register.

Similarly, Birrittella fails to provide any motivation to combine with Tanaka to provide the elements of the present invention. Birrittella discloses a system for improving the virtual addressing of vector data. The system significantly reduces the penalty of including virtual addressing in a computer system having a vector processor by allowing effective overlapped instruction execution during a vector memory-reference vector instruction. (column 2, lines 5-14). The problems addressed by Birrittella's system are handled by the processor, not by an operating system. As previously

mentioned, the problems that arise with respect to handling multiple programs are usually addressed at the operating system level. Therefore Birrittella, like Tanaka, fails to recognize the need to address the problems that arise when a second program attempts to transfer vector data between memory and a register.

Therefore, both Tanaka and Birrittella fail to recognize the need for, and so could not be expected to provide for, "generating a vector transfer unit exception if a second program attempts to transfer vector data between memory and a register of the register file via any vector buffer of the vector buffer pool, if a configuration register indicates that said vector buffer is in use," as recited in claim 53.

Applicant therefore respectfully submits that claim 53 clearly distinguishes over Tanaka in view of Birrittella. Applicant submits that these arguments apply with equal force to independent claims 66 and 77. Applicant therefore respectfully submits that independent claims 53, 66 and 77, as well as claims 54, 56-65, 67, 69-76, 78 and 80-88, which depend on claims 53, 66 and 77, are also allowable for at least the foregoing reasons. Applicant therefore respectfully requests withdrawal of the rejections based upon 35 U.S.C. §103(a). Accordingly, Applicant respectfully submits that claims 53-54, 56-67, 69-78 and 80-88 are in condition for allowance.

CONCLUSION

In view of the remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to telephone the undersigned at 512-439-5093.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on 6/1/04.

Attorney for Applicant(s) Date of Signature 6/1/04

Respectfully submitted,

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